

**GR8-1**

***Disclaimer****:*

*The development for this processor began December 24th, 2024. Documentation for it began January 4th, 2025. The information provided in this overview is subject to change until the processor architecture is fully assembled and tested. Another report will be available alongside this one. That report will include prototype information and branching ideas that will lead to the architecture described here for the ~~G2X8~~ GR8-1.*

There has been a renaming of the architecture, and the development goals have changed since this was first documented in January. The architecture has gone through a redesign that should allow for higher theoretical performance while facilitating design. The MMU and Stack have been dropped to allow for a simpler design, more akin to a RISC processor, which is the goal. I’ll be discussing the goal of the GR8-1 in terms of performance and laying the ground for the GR8-2.

*Fig. 1 - General overview of the processor layout.*

This version of the redesign will opt out of the 16bit register idea, while maintaining a similar layout to January’s design. The queue, wrongly named stack, will be removed. The purpose of said queue was to have the return address of the operation queued until it was executed. The result would then be handled by the now removed MMU. In contrast, this architecture will rely on executing a store instruction for the result to be returned. The GPR found in the last iteration would have been directly accessed by the decoder, in this case, the GPR is now accessed by the scheduler. It is also shown that the number of registers and their width have been reduced in half, mainly to reduce complexity.